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(54) **INTEGRATED CIRCUITRY, METHODS OF FORMING CAPACITORS, AND METHODS OF FORMING INTEGRATED CIRCUITRY COMPRISING AN ARRAY OF CAPACITORS AND CIRCUITRY PERIPHERAL TO THE ARRAY**

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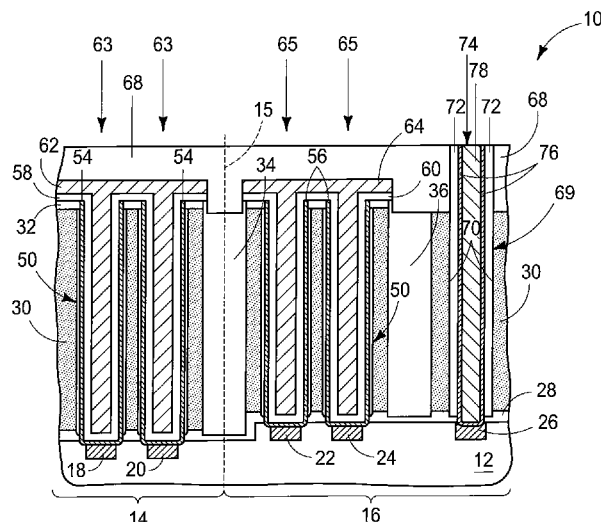
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**ABSTRACT**

A method of forming capacitors includes providing a support material over a substrate. The support material is at least one of semiconductive or conductive. Openings are formed into the support material. The openings include at least one of semiconductive or conductive sidewalls. An insulator is deposited along the semiconductive and/or conductive opening sidewalls. A pair of capacitor electrodes having capacitor dielectric there-between is formed within the respective openings laterally inward of the deposited insulator. One of the pair of capacitor electrodes within the respective openings is laterally adjacent the deposited insulator. Other aspects are disclosed, including integrated circuitry independent of method of manufacture.

**40 Claims, 6 Drawing Sheets**



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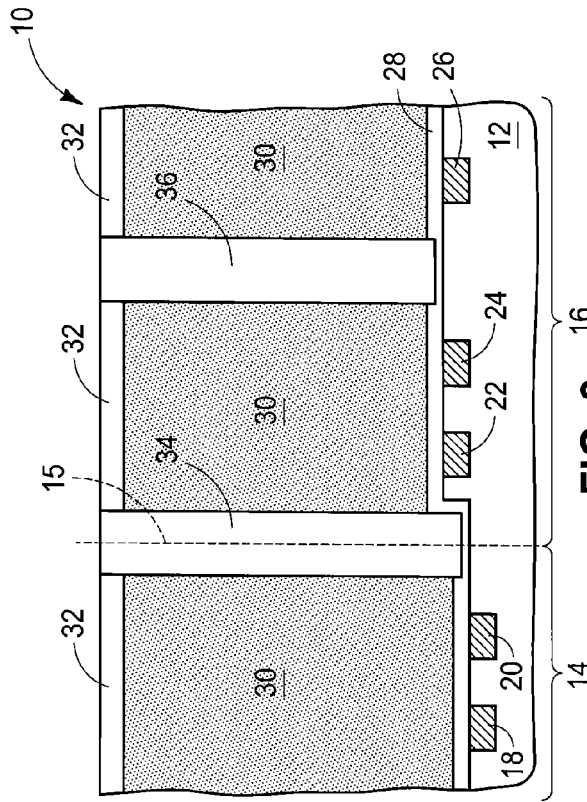


FIG. 1

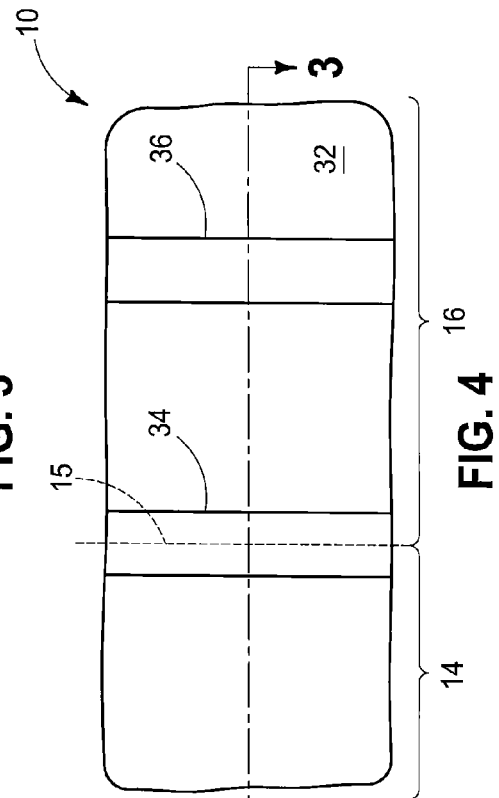


FIG. 2

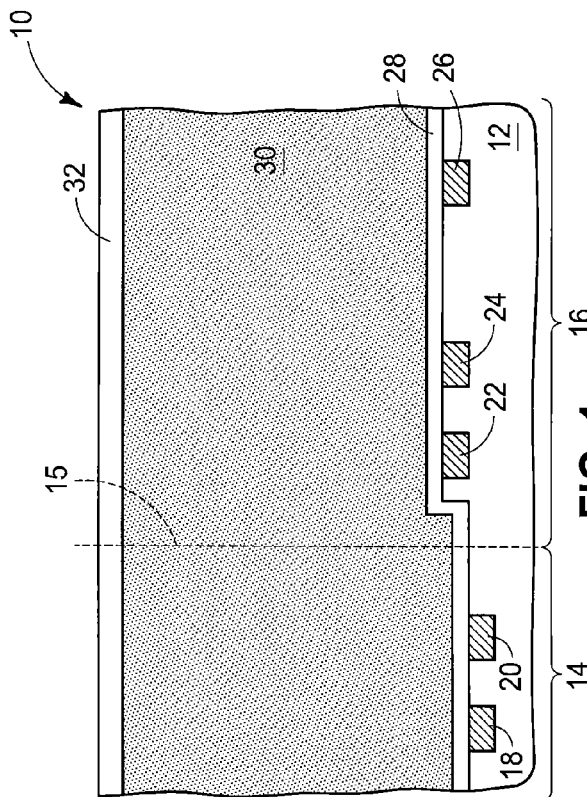


FIG. 3

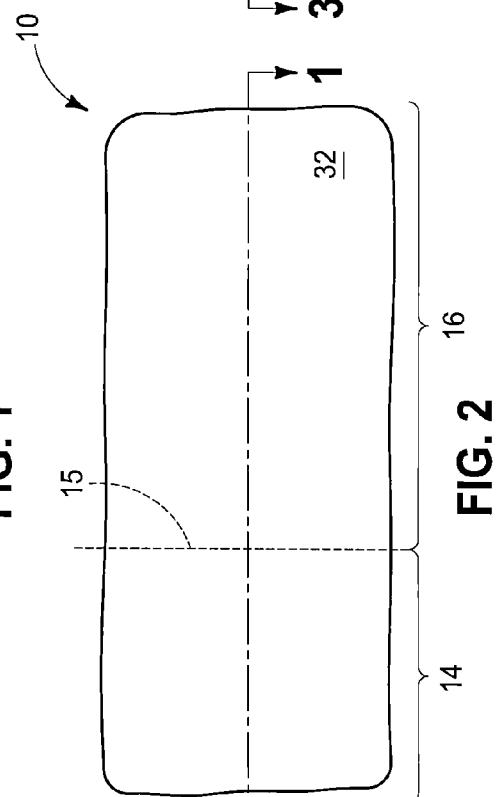
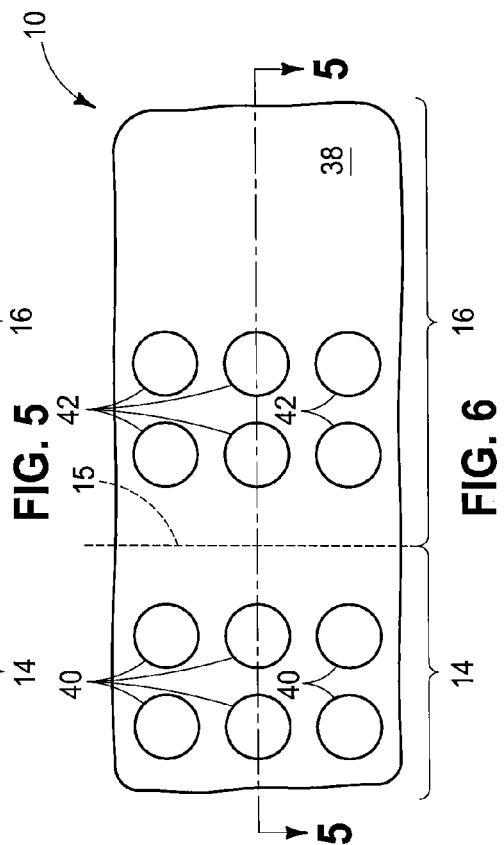
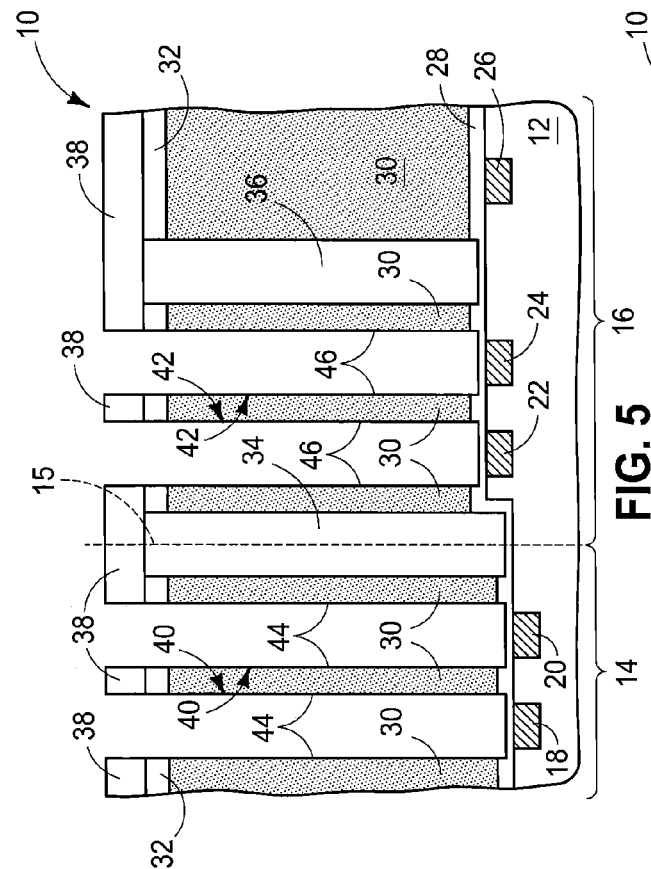
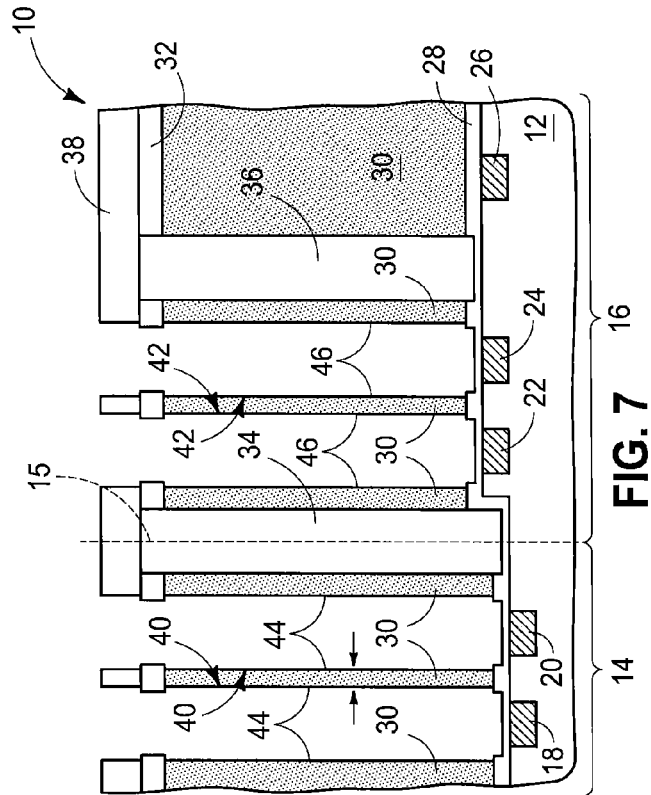
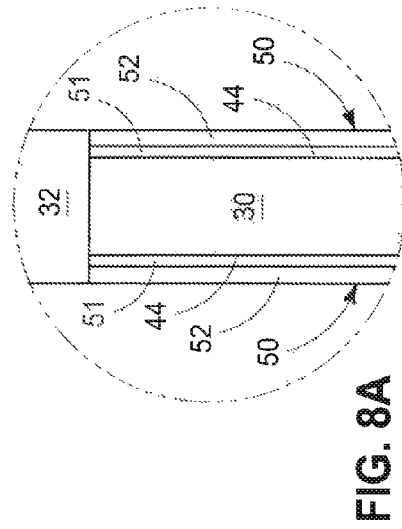
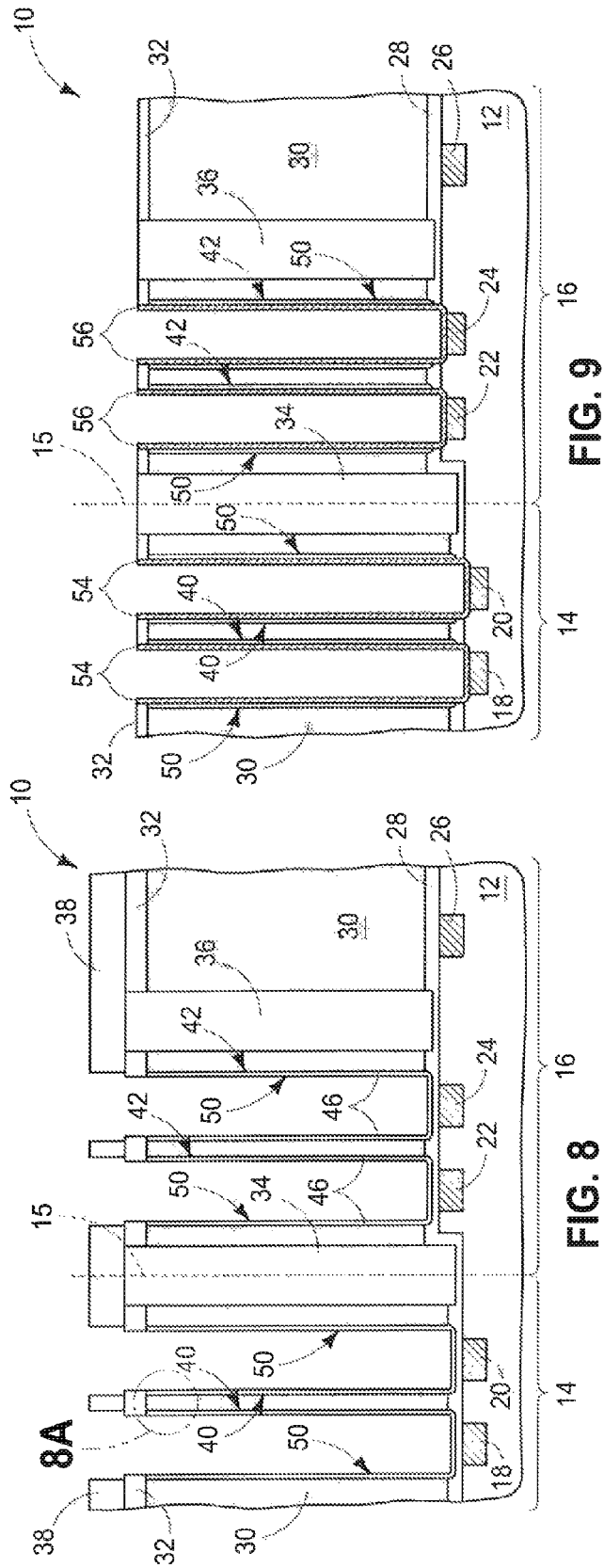
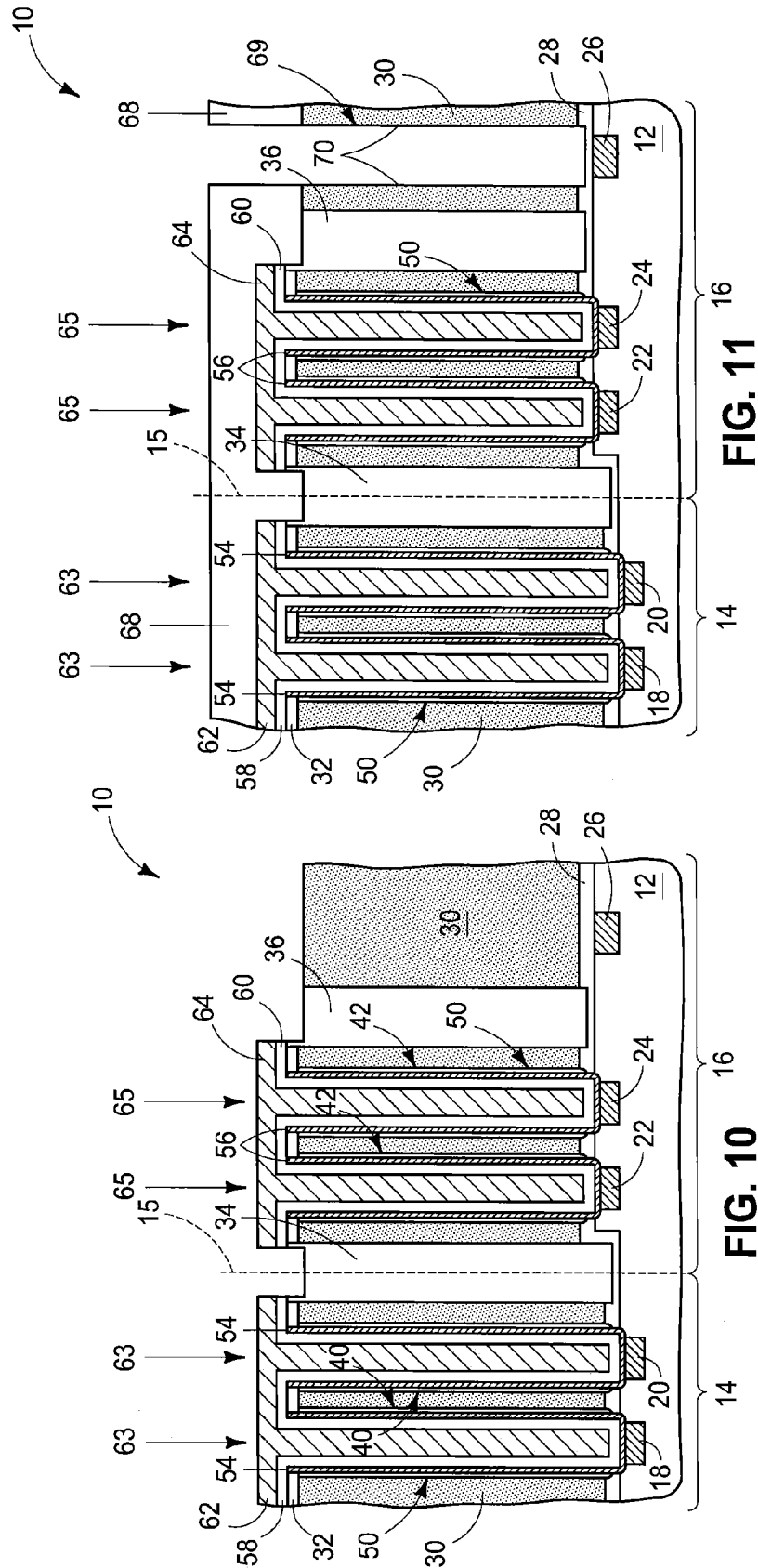


FIG. 4







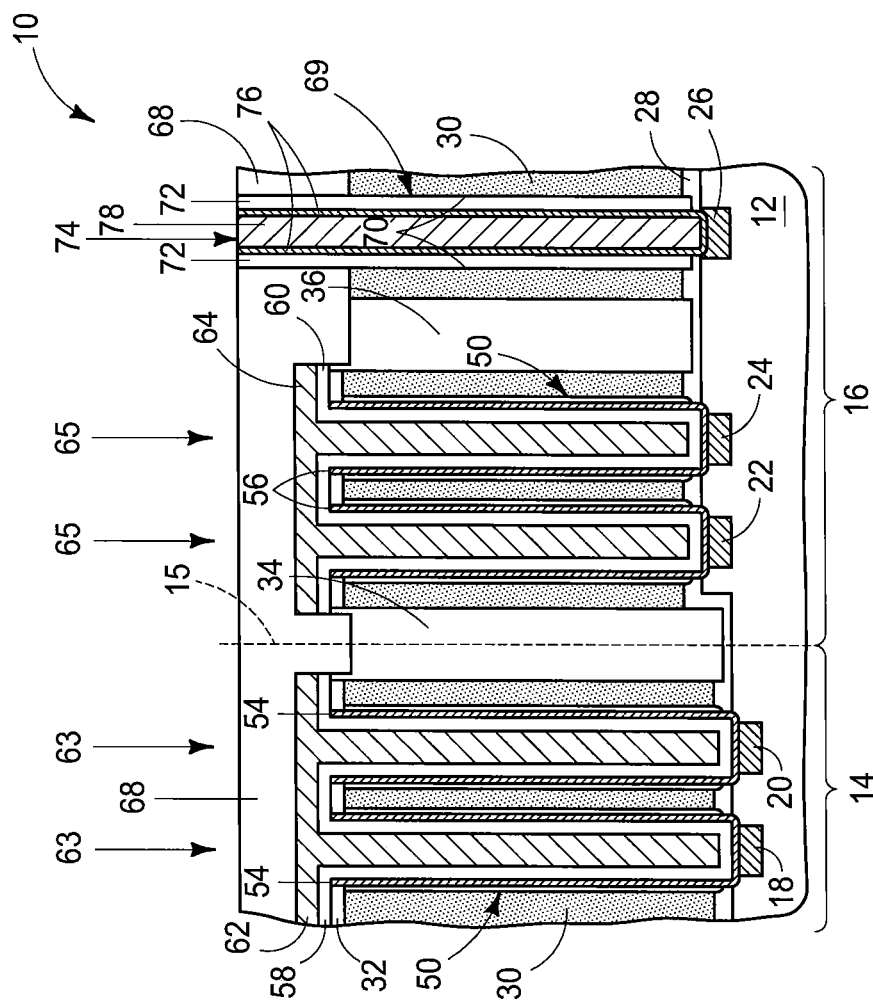
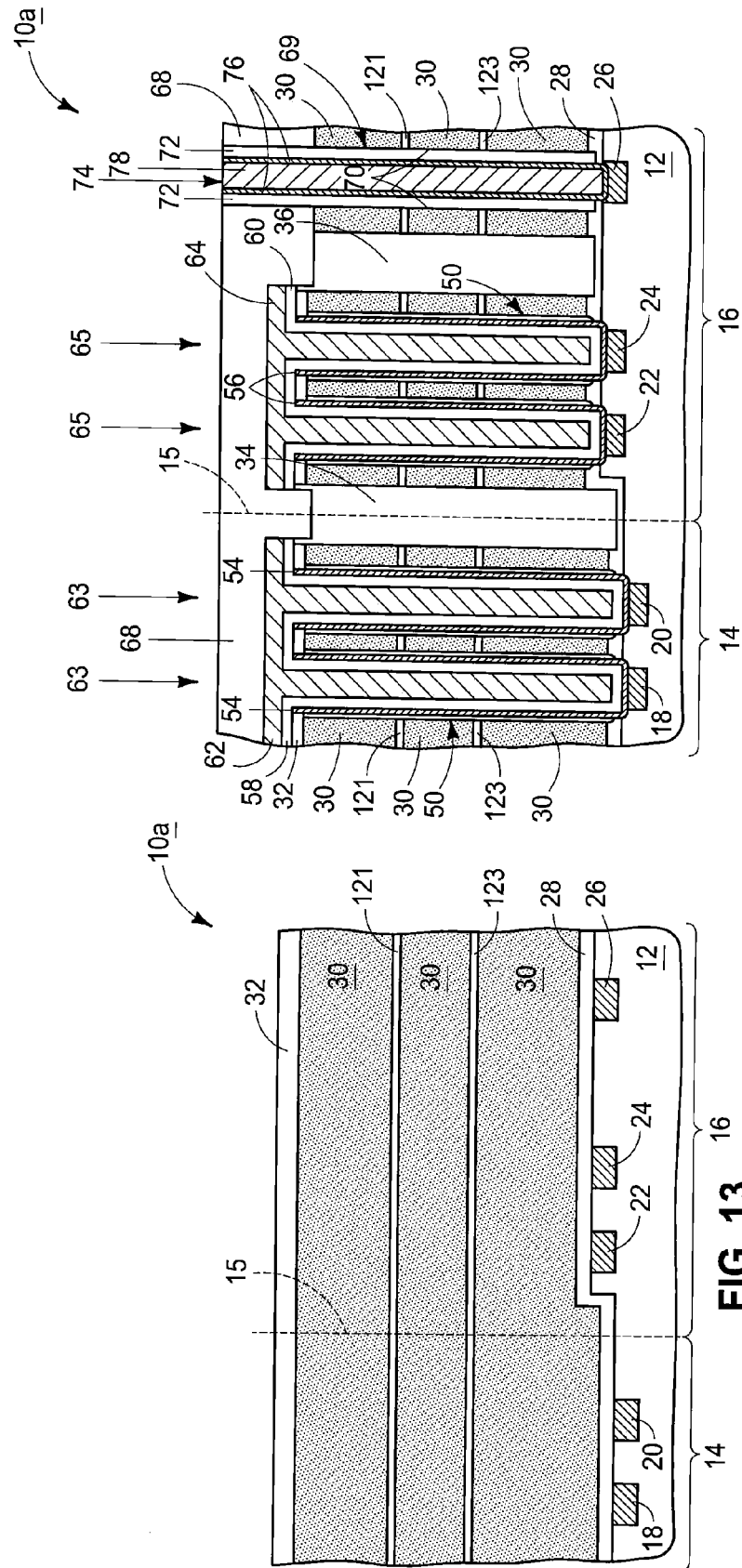


FIG. 12



1

# INTEGRATED CIRCUITRY, METHODS OF FORMING CAPACITORS, AND METHODS OF FORMING INTEGRATED CIRCUITRY COMPRISING AN ARRAY OF CAPACITORS AND CIRCUITRY PERIPHERAL TO THE ARRAY

## TECHNICAL FIELD

Embodiments disclosed herein pertain to integrated circuitry, and to methods of forming capacitors including methods of forming integrated circuitry comprising an array of capacitors and circuitry peripheral to the array.

## BACKGROUND

Capacitors are one type of component used in the fabrication of integrated circuits, for example in DRAM and other memory circuitry. A capacitor is comprised of two conductive electrodes separated by a non-conducting dielectric region. As integrated circuitry density has increased, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing capacitor area. The increase in density has typically resulted in greater reduction in the horizontal dimension of capacitors as compared to the vertical dimension. In many instances, the vertical dimension of capacitors has increased.

One manner of fabricating capacitors is to initially form an insulative material within which a capacitor storage electrode is formed. For example, an array of capacitor electrode openings for individual capacitors may be fabricated in an insulative support material, with an example material being silicon dioxide doped with one or both of phosphorus and boron. Openings within which some or all of the capacitors are formed are etched into the support material. It can be difficult to etch such openings through the support material, particularly where the openings are deep.

Further and regardless, it is often desirable to etch away most if not all of the capacitor electrode support material after individual capacitor electrodes have been formed within the openings. Such enables outer sidewall surfaces of the electrodes to provide increased area and thereby increased capacitance for the capacitors being formed. However, capacitor electrodes formed in deep openings are often correspondingly much taller than they are wide. This can lead to toppling of the capacitor electrodes, either during etching to expose the outer sidewall surfaces, during transport of the substrate, and during deposition of the capacitor dielectric layer and/or outer capacitor electrode layer. U.S. Pat. No. 6,667,502 teaches the provision of a brace or retaining structure intended to alleviate such toppling. Other aspects associated in the formation of a plurality of capacitors, some of which include bracing structures, are also disclosed and are:

U.S. Pat. No. 7,067,385;  
 U.S. Pat. No. 7,125,781;  
 U.S. Pat. No. 7,199,005;  
 U.S. Pat. No. 7,202,127;  
 U.S. Pat. No. 7,387,939;  
 U.S. Pat. No. 7,439,152;  
 U.S. Pat. No. 7,517,753;  
 U.S. Pat. No. 7,544,563;  
 U.S. Pat. No. 7,557,013;  
 U.S. Pat. No. 7,557,015;  
 U.S. Patent Publication No. 2008/0090416;  
 U.S. Patent Publication No. 2008/0206950;  
 U.S. Pat. No. 7,320,911;  
 U.S. Pat. No. 7,682,924; and  
 U.S. Patent Publication No. 2010/0009512.

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Fabrication of capacitors in memory circuitry may include forming an array of capacitors within a capacitor array area. Control or other circuitry area is often displaced from the capacitor array area, and the substrate may include an intervening area between the capacitor array area and the control or other circuitry area.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic, cross-sectional view of a portion of a semiconductor substrate at a preliminary processing stage of an embodiment in accordance with the invention.

FIG. 2 is a diagrammatic top view of a portion of the semiconductor substrate comprising the cross-section shown in FIG. 1 along the line 1-1.

FIG. 3 is a diagrammatic, cross-sectional view of the FIG. 1 substrate at a processing stage subsequent to that of FIG. 1.

FIG. 4 is a diagrammatic top view of the FIG. 3 substrate comprising the cross-section shown in FIG. 3 along the line 3-3.

FIG. 5 is a diagrammatic, cross-sectional view of the FIG. 3 substrate at a processing stage subsequent to that of FIG. 3.

FIG. 6 is a diagrammatic top view of the FIG. 5 substrate comprising the cross-section shown in FIG. 5 along the line 5-5.

FIG. 7 is a diagrammatic, cross-sectional view of the FIG. 5 substrate at a processing stage subsequent to that of FIG. 5.

FIG. 8 is a diagrammatic, cross-sectional view of the FIG. 7 substrate at a processing stage subsequent to that of FIG. 7.

FIG. 8A is an enlarged view of a portion of FIG. 8 showing the section shown in circle 8A in FIG. 8.

FIG. 9 is a diagrammatic, cross-sectional view of the FIG. 8 substrate at a processing stage subsequent to that of FIG. 8.

FIG. 10 is a diagrammatic, cross-sectional view of the FIG. 9 substrate at a processing stage subsequent to that of FIG. 9.

FIG. 11 is a diagrammatic, cross-sectional view of the FIG. 10 substrate at a processing stage subsequent to that of FIG. 10.

FIG. 12 is a diagrammatic, cross-sectional view of the FIG. 11 substrate at a processing stage subsequent to that of FIG. 11.

FIG. 13 is a diagrammatic, cross-sectional view of a portion of a semiconductor substrate at a preliminary processing stage of an embodiment in accordance with the invention.

FIG. 14 is a diagrammatic, cross-sectional view of the FIG. 13 substrate at a processing stage subsequent to that of FIG. 13.

## DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Some embodiments include methods of forming integrated circuitry comprising an array of capacitors and circuitry peripheral to the array. Some embodiments include methods of forming capacitors regardless of fabrication of integrated circuitry comprising both array and peripheral areas. Example methods of forming capacitors in accordance with embodiments of the invention are described with reference to FIGS. 1-12. Referring initially to FIGS. 1 and 2, a construction 10 is shown at a preliminary processing stage of an embodiment. Construction 10 includes a substrate 12 which may comprise semiconductive material. To aid in interpretation of the claims that follow, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies compris-

ing other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Construction 10 may comprise a capacitor array area 14 and a peripheral circuitry area 16. An example interface line 15 has been used in the drawings to define an interface of capacitor array area 14 and peripheral circuitry area 16. Logic circuitry may be fabricated within peripheral circuitry area 16. Control and/or other peripheral circuitry for operating a memory array may or may not be fully or partially within array area 14, with an example memory array area 14 as a minimum encompassing all of the memory cells of a given memory array/sub-memory array. Further, multiple sub-arrays might also be fabricated and operated independently, in tandem, or otherwise relative one another. As used herein, a "sub-array" or "sub-memory array" may be considered as an array. Various circuit devices (not shown) could be associated with peripheral circuitry area 16, as well as with capacitor array area 14, at the processing stage of FIGS. 1 and 2.

Electrically conductive node locations 18, 20 are shown within memory array area 14, and electrically conductive node locations 22, 24, 26 are shown within peripheral circuitry area 16. Node locations 18, 20, 22, 24, 26 may correspond to, for example, conductively-doped diffusion regions within a semiconductive material of substrate 12, and/or to conductive pedestals associated with substrate 12. Although the node locations are shown to be electrically conductive at the processing stage of FIG. 1, the electrically conductive materials of the node locations could be provided at a processing stage subsequent to that of FIG. 1 (not shown). The node locations may ultimately be electrically connected with transistor or other constructions (not shown), and can correspond to source/drain regions of transistor constructions, or can be ohmically connected to source/drain regions of transistor constructions. As an alternate example, the node locations may correspond to, connect to, or be parts of conductive interconnect lines.

Construction 10 may comprise dielectric material 28 elevationally over (i.e., atop) substrate 12 and/or node locations 18, 20, 22, 24, 26. Dielectric material 28 may be homogenous or non-homogenous, with silicon dioxide and silicon nitride being examples. An example thickness range for dielectric material 28 is from about 50 Angstroms to about 300 Angstroms.

A support material 30 is provided elevationally over substrate 12 within capacitor array area 14 and peripheral circuitry area 18. In one embodiment where dielectric material 28 is provided, support material 30 may be provided directly against dielectric material 28. In this document, a material or structure is "directly against" another when there is at least some physical touching contact of the stated materials or structures relative one another. In contrast, "over" encompasses "directly against" as well as constructions where intervening material(s) or structure(s) result(s) in no physical touching contact of the stated materials or structures relative one another. Regardless, support material 30 is at least one of semiconductive or conductive, and may be homogenous or non-homogenous. For example, support material 30 may be a single homogenous layer of a conductive or semiconductive material, multiple layers of a single homogenous semiconductive or conductive material, or multiple layers of differing compositions of semiconductive and/or conductive materials. An example support material comprises silicon, for example amorphous, monocrystalline, and/or polycrystalline silicon whether doped or undoped. One particular ideal material is

polycrystalline silicon which is either undoped to possess semiconductor properties, or lightly doped to possess semiconductor properties. As an alternate example, a polycrystalline silicon support material 30 may be heavily doped sufficiently to be electrically conductive. Additional example conductive materials include gallium nitride and carbon whether alone or in combination. An example thickness range for support material 30 is from about 2,500 Angstroms to about 3 microns.

A dielectric material 32 may be provided elevationally outward of (i.e. atop) semiconductive and/or conductive support material 30, and if provided may be directly against support material 30. Dielectric material 32 may be of the same composition or of different compositions from that of dielectric material 28. Dielectric material 32 may provide a chemical mechanical polishing stop, etch stop, and/or other function. An example thickness for dielectric material 32 is from about 600 Angstroms to about 1,500 Angstroms.

Referring to FIGS. 3 and 4, and in one embodiment, dielectric isolation 34 has been formed elevationally through (i.e., through the elevational thickness of) support material 30 to laterally separate capacitor array area 14 and peripheral circuitry area 16 from one another. In one embodiment and as shown, dielectric isolation 36 has also been formed elevationally through support material 30 within peripheral circuitry area 16. Dielectric isolation 34 and/or 36 when used may be formed at other times in the process, and regardless of when formed may be formed at the same time or at different times. Dielectric isolation 34, 36 may be of the same composition or of different compositions relative one another, may each be homogenous or non-homogenous, and may each be of the same composition or of different compositions from that of dielectric materials 28 and/or 32. An example technique for forming dielectric isolation 34 and/or 36 includes photolithographic patterning and etch through materials 32 and 30, and at least into dielectric material 28. Dielectric material 34 and/or 36 may then be deposited sufficiently to overfill the openings, followed by planarization back at least to the outermost surface of dielectric material 32 as shown. Where support material 30 is doped or undoped polysilicon, an example etching chemistry for anisotropically etching openings therein as shown includes  $\text{NF}_3:\text{O}_2:\text{HBr}$  at a volumetric ratio of 1:1:3 to 5. Alternate examples include substituting  $\text{SF}_6$  or  $\text{Cl}_2$  for the  $\text{NF}_3$  and in such events providing an alternate volumetric ratio of 1:1:1.

Referring to FIGS. 5 and 6, capacitor openings 40 have been formed into support material 30 within capacitor array area 14 and antifuse openings 42 have been formed into support material 30 within peripheral circuitry area 16. In one embodiment, capacitor openings 40 and/or antifuse openings 42 are formed completely through support material 30, as shown. An example technique for forming openings 40 and 42 includes photolithographic, or other masking, and etch of support material 30. For example, FIGS. 5 and 6 show a patterned hardmask 38 formed over support material 30. Openings have been etched through patterned mask 38 first through insulator material 32, with capacitor openings 40 and antifuse openings 42 within support material 30 then being formed. Etching may continue into dielectric material 28 to form openings either partially (as shown) or fully (not shown) therein or there-through. The openings that are formed in dielectric material 32 and 28 may align with openings 40, 42 in support material 30.

When both of capacitor openings 40 and antifuse openings 42 are ultimately formed, such may be formed in the same masking step (as shown) or in different masking steps. Regardless, capacitor openings 40 have at least one of semi-

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conductive or conductive sidewalls 44, and antifuse openings 42 have at least one of semiconductive or conductive sidewalls 46. Sidewalls 44 and 46 may comprise both a semiconductive portion and a conductive portion where, for example, support material 30 comprises a semiconductive portion elevationally inward (i.e., downward on the plane of the page upon which FIG. 5 lies) or elevationally outward (i.e., upward on the plane of the page upon which FIG. 5 lies) relative to a conductive portion. Alternately by way of example, sidewalls 44, 46 may be semiconductive if support material 30 along where the sidewalls are formed is only of one or more semiconductive materials or conductive if only of one or more conductive materials. Regardless, FIGS. 3-6 depict but one example embodiment wherein dielectric isolation 34, 36 has been formed before forming openings 40, 42, although isolation 34 and/or 36 could be formed later in the process.

Referring to FIG. 7, capacitor openings 40 within support material 30 and antifuse openings 42 within support material 30 have been laterally widened. Such may occur by any suitable method, for example by an isotropic etch which may be substantially selective to etch material 30 greater than any etching of material(s) 32 and/or 28. Where, for example, support material 30 comprises doped or undoped polysilicon and dielectric material(s) 28 and/or 32 comprise(s) silicon dioxide and/or silicon nitride, an aqueous HF solution may be used to isotropically etch material 30 as shown. Aqueous HF may also remove any native oxide that may be received over sidewalls 44 and/or 46. Such a solution may alternately, by way of example, be used to remove any such native oxide without appreciably etching support material 30 if conducted quickly enough. Regardless, in one embodiment, FIGS. 5 and 6 depict an example wherein first openings have been formed into support material, followed by laterally widening the first openings into wider second openings (FIG. 7). In one embodiment, the first openings may be formed by anisotropically etching of the support material and the laterally widening may be by isotropically etching the support material.

Referring to FIGS. 8 and 8A, an insulator 50 has been deposited along semiconductive and/or conductive capacitor opening sidewalls 44. Additionally, an insulator 50 has been deposited along semiconductive and/or conductive antifuse opening sidewalls 46. The insulators along sidewalls 44 and 46 may be of the same composition or of different compositions. Further and regardless, insulator 50 deposited along antifuse opening sidewalls 46 may be deposited while depositing insulator 50 along capacitor opening sidewalls 44. Insulator 50 may be formed directly against support material sidewalls 44 and/or 46.

Insulator 50 may be homogenous or non-homogenous, with an example thickness being from about 10 Angstroms to about 75 Angstroms. In the depicted example, insulator 50 is shown as comprising an insulative material 51 and an insulative material 52 (FIG. 8A). Materials 51 and 52 may be homogenous or non-homogenous, and may also be formed over dielectric material 28 at the base of capacitor openings 40 and antifuse openings 42 (as shown) and/or over sidewalls and tops of materials 32 and/or 38 (not shown). Regardless, in one embodiment, insulator 50 may be deposited by thermally oxidizing support material 30 of sidewalls 44 and 46. In one embodiment, depositing insulator 50 may comprise at least one of chemical vapor depositing or atomic layer depositing the insulator along sidewalls 44, 46. In one embodiment, insulative material 51 may be formed by thermally oxidizing the support material opening sidewalls 44, 46 followed by chemical vapor depositing and/or atomic layer depositing insulative material 52 laterally thereover. Where, for example, support material 30 comprises polysilicon, insula-

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tive material 50 may be thermally oxidized to form  $\text{SiO}_2$  in an ozone or other oxygen-containing ambient. An example ideal insulative material 52 is  $\text{Al}_2\text{O}_3$ . Regardless, an example lateral thickness for each of insulative materials 51 and 52 is from about 10 Angstroms to about 40 Angstroms. In one embodiment and as shown, insulative material 52 is thicker than insulative material 51. Additionally, more than two insulative material layers (not shown) may be used.

A pair of capacitor electrodes having a capacitor dielectric there-between is formed within the capacitor openings laterally of the deposited insulator. A pair of antifuse electrodes having insulative material there-between is formed within the respective antifuse openings laterally of the deposited insulator in the antifuse openings. Such capacitors and antifuses may be formed at the same time or at different times. FIG. 9 depicts an example embodiment wherein hard-mask material 38 (not shown) has been removed as have materials 50 and 28 that are over conductive node locations 18, 20, 22, and 24. Conductive material has then been deposited and planarized back to form elevationally inner capacitor electrodes 54 (e.g., first capacitor electrodes) and elevationally inner antifuse electrodes 56 (e.g., first antifuse electrodes) within openings 40 and 42, respectively. In one embodiment, the depicted electrodes 54 and/or 56 have upwardly open container-like shapes. An example conductive material is one or both of titanium and titanium nitride to provide at least electrodes 54 to have a minimum thickness, in one embodiment, of from about 20 Angstroms to about 50 Angstroms.

Referring to FIG. 10, an elevationally outer capacitor electrode 62 (e.g., a second capacitor electrode) and capacitor dielectric 58 have been formed over inner capacitor electrodes 54. An elevationally outer antifuse electrode 64 (e.g., a second antifuse electrode) and insulative material 60 have been formed over inner antifuse electrodes 56. Capacitors 63 and antifuses 65 are formed thereby. In one embodiment, one or both of outer capacitor electrode 62 and capacitor dielectric 58 is continuously received over multiple capacitor electrodes 54, with both being shown over multiple capacitor electrodes 54 in the depicted embodiment. In one embodiment, one or both of outer antifuse electrode 62 and antifuse insulative material 60 is continuously received over multiple antifuse electrodes 56, with both being shown over multiple capacitor electrodes 56 in the depicted embodiment. Dielectrics 58 and 60 may be homogenous or non-homogenous, may be of the same composition or of different compositions, and may be deposited at the same time or at different times. Conductive electrodes 62 and 64 may be homogenous or non-homogenous, may be of the same composition or of different compositions, and may be deposited and the same time or at different times. Regardless, one of the pair of the capacitor electrodes 54 or 62 within the respective capacitor openings 40 (i.e., electrode 54) is laterally adjacent to (in one embodiment directly against) deposited insulator 50 in capacitor openings 40. One of the pair of antifuse electrodes 56, 64 within the respective antifuse openings 42 (i.e., antifuse electrode 56) is laterally adjacent to (in one embodiment directly against) deposited insulator 50 in antifuse openings 42.

Appropriate circuitry (not shown) would be associated with electrodes 56 and 64 of antifuses 65 to enable selective programming of individual antifuses 65 (i.e., by breaking down/"blowing" dielectric material 60 within individual openings 42 to cause conductive material to bridge between outer electrode 64 and an individual inner electrode 56). Appropriate circuitry (not shown) would be associated with capacitor electrodes 54 and 62 of capacitors 63 to enable selective operation of individual capacitors 63 that would not

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include breaking down/"blowing" capacitor dielectric 58 to short electrodes 54 and 62 to one another. In other words, although an antifuse and a capacitor are each an electronic device, antifuses are not capacitors and capacitors are not antifuses in the context of this document. While each may be of the same or similar construction(s) having a pair of electrodes with dielectric there-between, other respective portions of the integrated circuitry would be configured to operate the electronic device either as an antifuse or a capacitor and thereby be determinative of device type. These other respective circuitry portions are not material to embodiments of this invention, and may be existing or later developed circuitry within the skill of the artisan.

Referring to FIG. 11, a dielectric 68 has been deposited and peripheral circuitry contact openings 69 (only one being shown) have been formed into support material 30 within peripheral circuitry area 16. Openings (only one being shown) have been formed through dielectric 68 prior to forming contact openings 69 within support material 30. Support material contact openings 69 have at least one of semiconductive or conductive sidewalls 70 analogous to that described above for sidewalls 44 and 46. Peripheral circuitry contact openings 69 may be formed before or after forming either of capacitor openings 40 and/or antifuse openings 42.

Referring to FIG. 12, an insulator 72 has been deposited along semiconductive and/or conductive contact opening sidewalls 70, and a conductive contact 74 has been formed within the respective contact openings 69 laterally of deposited insulator 72 within contact openings 69. In one embodiment, insulator 72 is directly against sidewalls 70, and in one embodiment insulator 72 is directly against conductive contact 74. Insulator 72 may have any of the attributes described above with respect to insulator 50 within capacitor openings 40 and insulator 50 within antifuse openings 42. Conductive contact 74 may be homogenous or non-homogenous, with an example conductive liner 76 and central plugging material 78 being shown (e.g., titanium nitride and tungsten, respectively).

The support material may be considered as having an elevationally outermost (i.e., a top) surface and an elevationally innermost (i.e., a bottom) surface. Some embodiments of the invention comprise providing at least one dielectric layer within conductive and/or semiconductive support material between the elevationally outermost and elevationally innermost surfaces of such support material. An example of such an embodiment is described with reference to FIGS. 13 and 14 with respect to a substrate construction 10a. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a" or with different numerals. FIG. 13 corresponds in processing sequence to FIG. 1 of the first-described embodiments. Two dielectric layers 121, 123 are provided within support material 30 between elevationally outermost and elevationally innermost surfaces of support material 30. Only one dielectric layer (not shown) or more than two dielectric layers (not shown) might be used. Regardless, the dielectric layer(s) may be homogenous or non-homogenous, and regardless may be of the same composition or of different compositions relative one another where more than one dielectric layer is provided. Further, the dielectric layer(s) may be continuous or discontinuous over the area where such are, and regardless may not be received within each of array area 14 and peripheral circuitry area 16. The dielectric layer(s) may be formed by alternating depositions of support material 30 and material(s) of the dielectric layer(s).

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FIG. 14 depicts construction 10a at a processing sequence corresponding to that of FIG. 12 of the first-described embodiments. Any of the processing and constructions described above in proceeding from FIG. 1 to FIG. 12 may be used in the embodiment of FIGS. 12 and 14.

In contradistinction to the embodiment of FIGS. 13 and 14, FIGS. 1-12 show processing and construction which is devoid of any dielectric layer within conductive and/or semiconductive support material between elevationally outermost and elevationally innermost surfaces of such support material.

Embodiments of the invention include any of the above constructions as shown and/or described independent of method of manufacture.

## CONCLUSION

In some embodiments, methods of forming capacitors comprise providing a support material over a substrate. The support material is at least one of semiconductive or conductive. Openings are formed into the support material. The openings comprise at least one of semiconductive or conductive sidewalls. An insulator is deposited along the semiconductive and/or conductive opening sidewalls. A pair of capacitor electrodes having capacitor dielectric there-between is formed within the respective openings laterally inward of the deposited insulator. One of the pair of capacitor electrodes within the respective openings is laterally adjacent the deposited insulator.

In some embodiments, methods of forming integrated circuitry comprising an array of capacitors and circuitry peripheral to the array comprise providing a support material over a substrate within a capacitor array area and within peripheral circuitry area. The support material is at least one of conductive or semiconductive. Capacitor openings are formed into the support material within the capacitor array area. The capacitor openings comprise at least one of semiconductive or conductive sidewalls. An insulator is deposited along the semiconductive and/or conductive capacitor opening sidewalls. A pair of capacitor electrodes having capacitor dielectric there-between is formed within the respective capacitor openings laterally inward of the deposited insulator in the capacitor openings. One of the pair of capacitor electrodes within the respective capacitor openings is laterally adjacent the deposited insulator in the capacitor openings. Contact openings are formed into the support material within the peripheral circuitry area. The contact openings comprise at least one of semiconductive or conductive sidewalls. An insulator is deposited along the semiconductive and/or conductive contact opening sidewalls. A conductive contact is formed within the respective contact openings laterally inward of the deposited insulator in the contact openings.

In some embodiments, methods of forming integrated circuitry comprising an array of capacitors and circuitry peripheral to the array comprise providing a support material over a substrate within a capacitor array area and within peripheral circuitry area. The support material is at least one of semiconductive or conductive. Capacitor openings are formed into the support material within the capacitor array area. The capacitor openings comprise at least one of semiconductive or conductive sidewalls. An insulator is deposited along the semiconductive and/or conductive capacitor opening sidewalls. A pair of capacitor electrodes having capacitor dielectric there-between is formed within the respective capacitor openings laterally inward of the deposited insulator. One of the pair of capacitor electrodes within the respective capacitor openings is laterally adjacent the deposited insulator in the capacitor openings. Antifuse openings are formed into the

support material within the peripheral circuitry area. The antifuse openings comprise at least one of semiconductive or conductive sidewalls. An insulator is deposited along the semiconductive and/or conductive antifuse opening sidewalls. A pair of antifuse electrodes having insulative material there-between is formed within the respective antifuse openings laterally inward of the deposited insulator in the antifuse openings. One of the pair of antifuse electrodes within the respective antifuse openings is laterally adjacent the deposited insulator in the antifuse openings.

In some embodiments, integrated circuitry includes a plurality of electronic devices which individually comprise a pair of conductive electrodes having dielectric there-between. The integrated circuitry includes a substrate comprising support material there-over. The support material is at least one of semiconductive or conductive. Electronic device openings extend into the support material, and comprise at least one of semiconductive or conductive sidewalls. An insulator is along the semiconductive and/or conductive electronic device opening sidewalls. Individual electronic devices are within individual of the electronic device openings laterally inward of the insulator that is along the semiconductive and/or conductive electronic device opening sidewalls. The electronic devices individually comprise a pair of conductive electrodes having dielectric there-between. One of the pair of conductive electrodes within the respective electronic device openings is laterally adjacent the deposited insulator.

In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

The invention claimed is:

1. A method of forming capacitors, comprising:  
forming a support material over a substrate, the support material being at least one of semiconductive or conductive;  
forming openings into the support material, the openings comprising at least one of semiconductive or conductive sidewalls;  
depositing an insulator within the openings along the sidewalls that are at least one of semiconductive or conductive;  
after depositing the insulator, depositing conductive material for a first capacitor electrode within individual of the openings; the conductive material for the first capacitor electrode within the individual openings being laterally adjacent to the insulator;  
after depositing the conductive material for the first capacitor electrodes, depositing capacitor dielectric material within the individual openings over the conductive material for the first capacitor electrode that is within the individual openings; and  
depositing conductive material for a second capacitor electrode within the individual openings over the capacitor dielectric material that is within the individual openings, the insulator being absent between the first and second capacitor electrodes within the individual openings.
2. The method of claim 1 wherein the support material and the support material opening sidewalls are semiconductive.
3. The method of claim 1 wherein the support material and the support material opening sidewalls are conductive.

4. The method of claim 1 wherein the support material comprises a semiconductive portion and a conductive portion, and the opening sidewalls comprise a semiconductive portion and a conductive portion.

5. The method of claim 1 wherein the support material comprises silicon.

6. The method of claim 5 wherein the silicon is amorphous.

7. The method of claim 5 wherein the silicon is monocrystalline.

8. The method of claim 5 wherein the silicon is polycrystalline.

9. The method of claim 8 wherein the polycrystalline silicon is undoped.

10. The method of claim 8 wherein the polycrystalline silicon is doped.

11. The method of claim 1 wherein the support material comprises at least one of gallium nitride and carbon.

12. The method of claim 1 wherein the openings are formed completely through the support material.

13. The method of claim 1 comprising forming dielectric material that is at least one of atop or under the support material and which is directly against the support material, openings being formed into the dielectric material which align with the openings in the support material.

14. The method of claim 1 wherein the depositing of the insulator comprises thermally oxidizing the support material of the opening sidewalls.

15. The method of claim 1 wherein the depositing of the insulator comprises at least one of chemical vapor depositing or atomic layer depositing the insulator along the opening sidewalls.

16. The method of claim 1 wherein the depositing of the insulator comprises:

thermally oxidizing the support material of the opening sidewalls; and

at least one of chemical vapor depositing or atomic layer depositing dielectric material laterally over the thermally oxidized support material.

17. The method of claim 1 wherein forming the openings comprises:

forming first openings into the support material; and  
laterally widening the first openings into wider second openings along which the insulator is deposited.

18. The method of claim 17 wherein forming the first openings comprises anisotropically etching the support material and the laterally widening comprises isotropically etching the support material.

19. The method of claim 1 comprising providing at least one dielectric layer within the support material between top and bottom surfaces of the support material.

20. The method of claim 1 being devoid of any dielectric layer within the support material between top and bottom surfaces of the support material.

21. A method of forming integrated circuitry comprising an array of capacitors and circuitry peripheral to the array, comprising:

forming support material over a substrate within a capacitor array area and within peripheral circuitry area, the support material being at least one of conductive or semiconductive;

forming capacitor openings into the support material within the capacitor array area, the capacitor openings comprising at least one of semiconductive or conductive sidewalls;

depositing an insulator within the capacitor openings along the capacitor opening sidewalls that are at least one of semiconductive or conductive;

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after depositing the insulator, depositing conductive material for a first capacitor electrode within individual of the capacitor openings; the conductive material for the first capacitor electrode within the individual capacitor openings being laterally adjacent to the insulator;

after depositing the conductive material for the first capacitor electrodes, depositing capacitor dielectric material within the individual capacitor openings over the conductive material for the first capacitor electrode that is within the individual capacitor openings;

depositing conductive material for a second capacitor electrode within the individual capacitor openings over the capacitor dielectric material that is within the individual capacitor openings, the insulator being absent between the first and second capacitor electrodes within the individual capacitor openings;

forming contact openings into the support material within the peripheral circuitry area, the contact openings comprising at least one of semiconductive or conductive sidewalls;

depositing insulative material within the contact openings along the contact opening sidewalls that are at least one of semiconductive or conductive; and

forming a conductive contact within individual of the contact openings radially inward of the deposited insulative material in the contact openings.

**22.** The method of claim **21** comprising forming dielectric isolation through elevational thickness of the support material and which laterally separates the capacitor array area and the peripheral circuitry area from one another.

**23.** The method of claim **22** wherein the dielectric isolation is formed before forming the capacitor openings.

**24.** The method of claim **21** wherein,

the insulative material is deposited directly against the contact opening sidewalls that are at least one of semiconductive or conductive; and

the conductive contact is formed directly against the deposited insulative material.

**25.** A method of forming integrated circuitry comprising an array of capacitors and circuitry peripheral to the array, comprising:

forming support material over a substrate within a capacitor array area and within peripheral circuitry area, the support material being at least one of semiconductive or conductive;

forming capacitor openings into the support material within the capacitor array area, the capacitor openings comprising at least one of semiconductive or conductive sidewalls;

forming antifuse openings into the support material within the peripheral circuitry area, the antifuse openings comprising at least one of semiconductive or conductive sidewalls;

depositing an insulator within the capacitor openings along the capacitor opening sidewalls that are at least one of semiconductive or conductive and within the antifuse openings along the antifuse opening sidewalls that are at least one of semiconductive or conductive;

after depositing the insulator, depositing conductive material for a first capacitor electrode within individual of the capacitor openings and for a first antifuse electrode within individual of the antifuse openings; the conductive material for the first capacitor electrode within the individual capacitor openings being laterally adjacent to the insulator; the conductive material for the first antifuse electrode within the individual antifuse openings being laterally adjacent to the insulator;

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after depositing the conductive material for the first capacitor electrodes and the first antifuse electrodes, depositing dielectric material within the individual capacitor openings over the conductive material for the first capacitor electrode that is within the individual capacitor openings and within the individual antifuse openings over the conductive material for the first antifuse electrode that is within the individual antifuse openings;

depositing conductive material for a second capacitor electrode within the individual capacitor openings over the dielectric material that is within the individual capacitor openings and for a second antifuse electrode within the individual antifuse openings over the dielectric material that is within the individual antifuse openings, the insulator being absent between the first and second capacitor electrodes within individual openings, and not being between the first and second antifuse electrodes within individual openings.

**26.** The method of claim **25** comprising:

forming contact openings into the support material within the peripheral circuitry area, the contact openings comprising at least one of semiconductive or conductive sidewalls;

depositing insulative material within the contact openings along the contact opening sidewalls that are at least one of semiconductive or conductive; and

forming a conductive contact within individual of the contact openings radially inward of the deposited insulative material in the contact openings.

**27.** The method of claim **26** wherein the contact openings, the insulative material along the contact opening sidewalls, and the conductive contacts are formed after depositing the conductive material for the second capacitor electrode within the individual capacitor openings over the dielectric material that is within the individual capacitor openings and for the second antifuse electrode within the individual antifuse openings over the dielectric material that is within the individual antifuse openings.

**28.** The method of claim **25** comprising forming dielectric isolation through elevational thickness of the support material and which laterally separates the capacitor array area and the peripheral circuitry area from one another, the dielectric isolation being formed before depositing the conductive material for the first capacitor electrode within individual of the capacitor openings and for the first antifuse electrode within individual of the antifuse openings.

**29.** The method of claim **28** comprising forming the dielectric isolation before forming the capacitor and antifuse openings.

**30.** The method of claim **1** wherein the conductive material for the first capacitor electrode is deposited within the individual openings directly against the insulator.

**31.** The method of claim **1** wherein the deposited insulator is deposited in two depositions, a first-deposited portion of the two depositions being thinner than a second-deposited portion of the two depositions.

**32.** The method of claim **1** wherein the deposited insulator is deposited in two depositions, a first-deposited portion of the two depositions being of different composition from a second-deposited portion of the two depositions.

**33.** The method of claim **32** wherein the first-deposited portion of the two depositions is thinner than the second-deposited portion of the two depositions.

**34.** The method of claim **1** wherein the insulator is also deposited over a base of the individual openings.

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35. The method of claim 34 comprising removing the insulator from being over the opening bases before depositing the conductive material for the first capacitor electrodes.

36. The method of claim 34 wherein the deposited insulator is not atop any of the bases in a finished circuitry construction incorporating the capacitors.

37. The method of claim 1 further comprising forming a first dielectric material between the support material and a conductive node underlying individual of the openings, and wherein forming the openings extends the openings through the support material and only partially into the first dielectric material, the insulator extending only partially into the first dielectric material in a finished circuitry construction incorporating the capacitors, the first capacitor electrodes electrically coupling with individual of the conductive nodes.

38. The method of claim 37 wherein depositing the insulator comprises depositing the insulator over a base of the dielectric material within individual of the openings, followed by removing a portion of the insulator from being over the bases, followed by removing a portion of the first dielectric material to expose the node locations, and followed by depositing the conductive material of the first capacitor electrode.

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39. The method of claim 1 wherein the first dielectric material is between the support material and a conductive node underlying individual of the openings and further comprising a second dielectric material is elevationally over an elevationally outermost surface of the support, and wherein the forming the openings extend the openings through the second dielectric material and the support material and only partially into the first dielectric material, the insulator extending only partially into the first dielectric material in a finished circuitry construction incorporating the capacitors, the insulator not extending into any of the second dielectric material in the circuitry construction, the first capacitor electrodes electrically coupling with individual of the conductive nodes.

40. The method of claim 39 wherein depositing the insulator comprises depositing the insulator over a base of the first dielectric material within individual of the openings, followed by removing a portion of the insulator from being over the bases, followed by removing the a portion of the first dielectric material to expose the node locations, and followed by depositing the conductive material of the first capacitor electrode.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 9,076,680 B2  
APPLICATION NO. : 13/276125  
DATED : July 7, 2015  
INVENTOR(S) : Brett W. Busch et al.

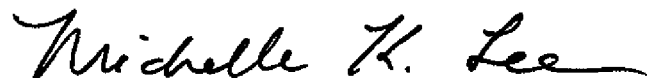
Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claims

Column 14, line 18, Claim 40 – Replace “removing the a portion” with --removing a portion--

Signed and Sealed this  
Seventeenth Day of November, 2015

A handwritten signature in black ink, reading "Michelle K. Lee". The signature is written in a cursive style with a long, sweeping underline.

Michelle K. Lee  
*Director of the United States Patent and Trademark Office*